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Fabrication of Ge-on-insulator wafers by Smart-Cut™ with thermal management for undamaged donor Ge wafers

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Abstract

Newly engineered substrates consisting of semiconductor-on-insulator are gaining much attention as starting materials for the subsequent transfer of semiconductor nanomembranes via selective etching of the insulating layer. Germanium-on-insulator (GeOI) substrates are critically important because of the versatile applications of Ge nanomembranes (Ge NMs) toward electronic and optoelectronic devices. Among various fabrication techniques, the Smart-Cut™ technique is more attractive than other methods because a high temperature annealing process can be avoided. Another advantage of Smart-Cut™ is the reusability of the donor Ge wafer. However, it is very difficult to realize an undamaged Ge wafer because there exists a large mismatch in the coefficient of thermal expansion among the layers. Although an undamaged donor Ge wafer is a prerequisite for its reuse, research related to this issue has not yet been reported. Here we report the fabrication of 4-inch GeOI substrates using the direct wafer bonding and Smart-Cut™ process with a low thermal budget. In addition, a thermo-mechanical simulation of GeOI was performed by COMSOL to analyze induced thermal stress in each layer of GeOI. Crack-free donor Ge wafers were obtained by annealing at 250 °C for 10 h. Raman spectroscopy and x-ray diffraction (XRD) indicated similarly favorable crystalline quality of the Ge layer in GeOI compared to that of bulk Ge. In addition, Ge p-n diodes using transferred Ge NM indicate a clear rectifying behavior with an on and off current ratio of 500 at ±1 V. This demonstration offers great promise for high performance transferrable Ge NM-based device applications.

Supplementary material for this article is available online

Keywords: Smart-Cut, germanium on insulator, semiconductor nanomembrane transfer

(Some figures may appear in colour only in the online journal)

Introduction

In recent years, research on semiconductor nanomembrane (NM) transfer by elastomeric polydimethylsiloxane (PDMS) stamps has been attracting intensive interest due to its versatile applications toward unconventional electronic and optoelectronic devices. This technique has been applied to transfer various types of semiconductor NMs such as Ge, GaAs, and 4H-SiC NM [1–3]. Among these materials, Ge has been intensively studied as a material platform for Si-compatible electronic or optoelectronic applications [4, 5]. Germanium on insulator (GeOI) substrates have been fabricated

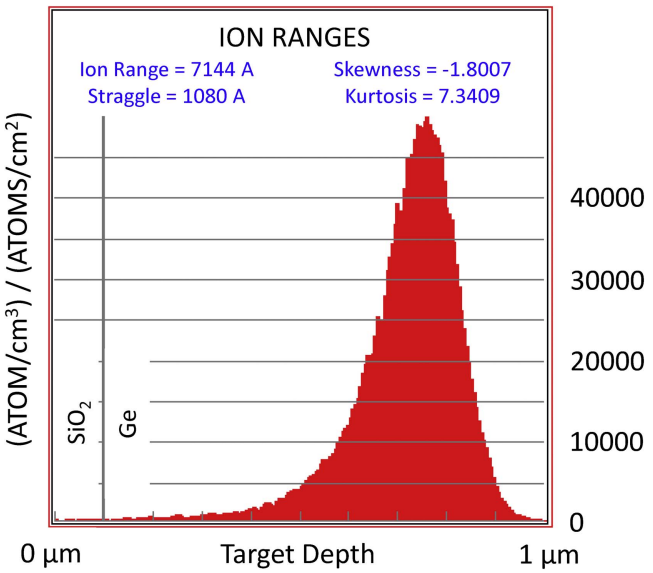

Figure 1. A simulated H^+ ion profiles on oxide-coated Ge wafer.

using various methods such as rapid melting growth and hetero-epitaxial growth techniques. Although single crystalline Ge films can be obtained, each of these methods are subject to their limitations. For example, the rapid melting growth method introduces a high temperature annealing (>800 °C) process to recrystallize the Ge material [6]. Hetero-epitaxy followed by a wafer transfer method requires substrate removal after wafer bonding [7]. Smart-Cut™ is more attractive than other methods because the high temperature annealing process can be circumvented [8]. High temperature annealing required for rapid melting growth and hetero-epitaxial growth can deteriorate the material quality of Ge such as hole mobility and surface roughness. Another advantage of Smart-Cut™ is that the Ge wafer can be reclaimed for the subsequent layer split process. It is very difficult to ensure the safety of the Ge wafers because the bonded Ge wafer is fragile during annealing, attributed to the large mismatch of the coefficient of thermal expansion (CTE) between Ge, Si, and SiO_2 (Ge: 5.9×10^{-6}/°C, Si: 2.6×10^{-6}/°C, and SiO_2: 5×10^{-7}/°C at room temperature) [9]. Larger diameter Ge wafers are more vulnerable to thermal stress. In this work, we realized 4-inch GeOI substrates entirely covered by Ge film and safe Ge donor wafers after the Smart-Cut™ technique via careful control of the annealing conditions. The demonstration indicated that Ge donor wafers can be claimed for reuse, which proves advantages of the Smart-Cut™ technique. As a proof-concept of the device, we fabricated vertical Ge p-n junction diodes using transferrable Ge NMs released from lab-made GeOI wafers.

Experiment

The process began with 4-inch bulk Ga doped p-type Ge wafers with a resistivity of 0.01 ~ 0.04 Ω-cm. A layer of SiOx of 100 nm thick was deposited on the Ge wafers by using plasma enhanced chemical vapor deposition (PECVD) to obtain a uniform ion implantation depth. The SiOx-capped Ge wafers were ion implanted at room temperature with a dose of 1×10^{17} cm^{-2} at 100 keV for the hydrogen (H^+) ion peak located at 660 nm underneath the top surface. Si wafers were oxidized by dry oxidation (TYSTAR furnace) at 1050 °C to grow 150 nm SiO_2 as the buried oxide (BOX) layer of the handling substrate for the final GeOI structure. The oxide layer on the Ge wafer was completely removed by hydrofluoric acid (HF, 49%) before the direct wafer bonding of the implanted Ge and oxidized Si wafers. Before wafer bonding, SC1 cleaning (NH_4OH:H_2O_2:H_2O 1:1:5, no H_2O_2 for Ge) and oxygen plasma activation (O_2: 50 sccm, RF power: 30 W, pressure: 50 mTorr) were performed on both the Ge and the oxidized Si wafers to enhance the bonding strength [10]. The wafers were immediately loaded into wafer bonder (EVG 501) chambers and aligned manually by quartz alignment pins. The chamber was pumped down to approximately 5×10^{-5} mbar and the bonding was initiated by applying an electrode force of 1000 N at room temperature. Bonded wafers were annealed at 100 °C *in situ* to improve the bonding strength. The effect of annealing temperature on exfoliation of Ge and fracture of Ge wafers was investigated by various annealing temperatures, namely 200, 250, 300, and 350 °C with a ramp up/down of 1 °C min^{-1}. The bonded wafer was annealed for 10 h in a nitrogen ambient. Chemical and mechanical polishing (CMP) was used to remove the damaged layer of the transferred Ge film. A systematic thermodynamic analysis of the GeOI (i.e., Ge-SiO_2-Si structure) was performed by the finite element modeling based on the multi-physics simulator, COMSOL. The maximum stress value that this structure can tolerate was calculated and compared to the thermally induced stress of the Ge-SiO_2-Si structure under different annealing temperatures. The cross-section of the GeOI was investigated by scanning electron microscopy (SEM, LEO 1530). The surface topology and crystal quality of the transferred Ge film were investigated by atomic force microscopy (AFM, Park Systems), Raman spectroscopy (Horiba LabRAM ARAMIS), and x-ray diffraction (XRD, PANalytical X'Pert PRO x-ray diffractometer).

Results and discussion

The implantation condition was obtained by using the simulation tool, Stopping and Range of Ions in Matter (SRIM) simulator. Figure 1 shows the H^+ ion profile in Ge wafers after the implantation of H^+ with a dose of 1×10^{17} cm^{-2} at 100 keV. The depth of the implanted H^+ ion peak was determined to be 660 nm to minimize structural damage in Ge films with a final thickness of 300 nm. It was reported that implanted H^+ ions leak out and delays in the post annealing process on the bonded wafer result in failure of exfoliation [11]. Therefore, all wafer bonding and subsequent annealing processes were completed within one week after H^+ implantation to avoid the leakage of H^+ ions. Since Ge, Si, and SiO_2 have different coefficients of CTE, a careful temperature control with slow ramp up/down (1 °C min^{-1}) was

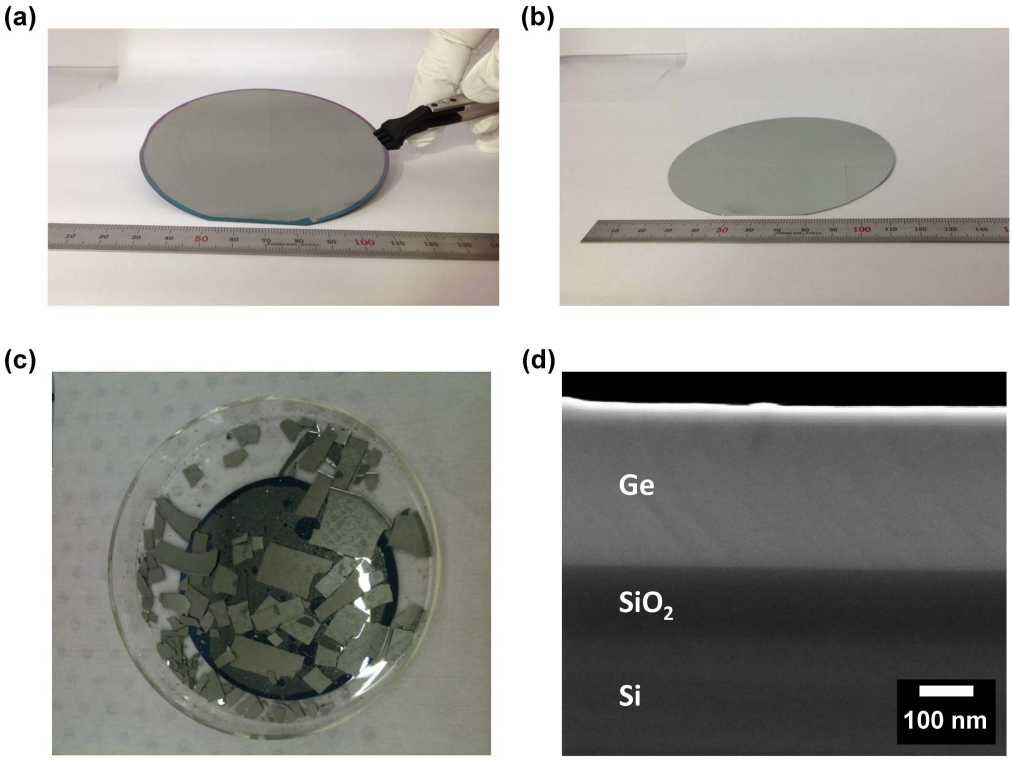

Figure 2. Photographs of (a) fabricated GeOI, (b) preserved donor Ge wafer after Smart-Cut^{TM} process and (c) broken donor Ge wafer after annealing at 300 °C for 10 h. (d) Cross-sectional SEM image of the fabricated GeOI.

necessary to avoid any damage on Ge wafers during annealing. In addition, a two-step low temperature anneal enhanced the nucleation of hydrogen platelets and completed the exfoliation.

In order to investigate the effect of anneal temperature on donor Ge wafers, we annealed the bonded wafers at various temperatures. While a low temperature annealing (i.e., 200 °C) resulted in failed exfoliation of Ge due to insufficient blister formation inside the bulk Ge wafer, high temperature annealing (i.e., 300 and 350 °C) makes the bonded bulk Ge wafer fracture into small pieces by induced thermal stress due to differences in CTE. Eventually, 660 nm thick Ge film was successfully transferred and the Ge donor wafer was also preserved after the 1st anneal at 200 °C for 3 h and the 2nd anneal at 250 °C for 10 h. Annealing at temperatures higher than 250 °C was effective to exfoliate Ge, but donor Ge wafers were fractured due to excessive thermal stress. Figure 2 shows the image of the fabricated GeOI (figure 2(a)), the preserved (figure 2(b)), and the broken Ge donor wafers (figure 2(c)) after Smart-Cut^{TM} process. Figure 2(d) shows a cross-sectional SEM image of the GeOI wafer after CMP. Thickness of the Ge and BOX layer was measured to be 300 and 150 nm, respectively, which corresponds well to the target thickness of each layer.

A thermo-mechanical simulation of GeOI under different annealing conditions was carried out by the finite element modeling based on the multi-physics simulator, COMSOL. In order to simulate the actual stress to GeOI during the annealing process, the time-dependent solution was used to calculate the von Mises thermal stress developed in the multilayered structure of GeOI, which consists of a 500 μm thick 4-inch Ge and Si wafer and a 150 nm SiO_2 sandwiched between two wafers, under annealing at different temperatures namely, 250, 300, and 350 °C. The initial temperature of the wafer was set to 20 °C. Experimental studies of the effect of temperature ramp rate on induced thermal stress have been reported [12]. It is noted that a faster temperature ramp rate leads to higher thermal stresses due to a very sharp increase in stress at the wafer's edge. Therefore, a slow ramp rate of 1 °C min^{-1} was used in the experiment to avoid possible thermal shock. The actual ramp rate (i.e., 1 °C min^{-1}) was applied in the simulation by a constant heat flux of 13.532 W m^{-2} to the structure at all the outer boundaries. The thermal stress generated in the structure between two temperatures T_1 and T_2 can be calculated by $\sigma_T = [E/(1-\nu)] \cdot (\alpha_{Ge} - \alpha_{Si}) \cdot (T_2 - T_1)$ [13], where σ_T is the thermal stress, $E/(1-\nu)$ is a biaxial elastic modulus of a Ge substrate, α_{Ge} and α_{Si} are CTE of Ge and Si substrates, and T_1 and T_2 are the initial and final temperatures. Figure 3(a) shows the three-dimensional stress distribution at 250 °C. As summarized in figure 3(b), the simulation results show the thermal stress developed in the wafer were 154, 188, and 221 MPa at 250, 300, and 350 °C, respectively. The simulation results indicate warpage in the wafer due to different CTE values for Si and Ge (Si: 2.6×10^{-6}/°C, Ge: 5.9×10^{-6}/°C). Since the Ge side of the Ge-SiO_2-Si structure is mainly responsible for the fracture, the fracture strength of the Ge was calculated from the fracture toughness of the Ge [14]. Fracture strength of the material is proportional to fracture toughness by the following relationship:

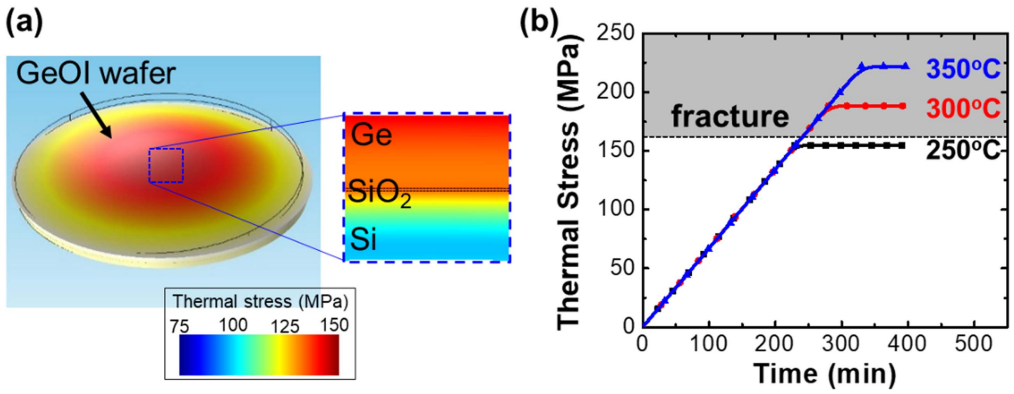

Figure 3. (a) A three-dimensional stress distribution of GeOI wafer at 250 °C. The zoomed-in image shows the stress distribution at the center of GeOI. (b) Simulated thermal stress under different temperatures (250, 300, and 350 °C) as a function of time, indicating that stress above 160 MPa will crack the Ge wafer.

$\sigma_T = K/f$ where K is the fracture toughness and f is the dimensional factor. Using experimental parameters (i.e., K [15] and σ_T [16] of Si: 0.7 MPa · $m^{1/2}$ and 220 MPa and K [17] of Ge: 0.51 MPa · $m^{1/2}$), the fracture strength of Ge was calculated to be 160 MPa. Therefore, as shown in figure 3(b), any stress above 160 MPa will crack the GeOI wafer which agrees well with the experiment conditions of GeOI fabrication.

Although the high temperature anneal may be effective for a short time exfoliation process, this will induce high thermal stress which results in breakage of wafers. It should be noted that a 200 °C anneal for 100 h failed to split the Ge layer from the donor Ge wafer. We believe that 200 °C is too low to complete the exfoliation process [8]. It was found that annealing at 250 °C for 10 h was the optimum recipe for both complete thin Ge film transfer and safe donor Ge wafer under our H^+ implant conditions. As shown in figure S1, available online at stacks.iop.org/SST/33/015017/mmedia, a root-mean-square (RMS) surface roughness of exfoliated Ge layer was measured to be 22.7 nm which is not immediately suitable for further device fabrication. The surface was polished to obtain a smooth surface with a RMS surface roughness of 0.7 nm, while reaching a final Ge thickness of 300 nm.

A Horiba LabRAM ARAMIS Raman confocal microscope with 100× objective with He-Ne (541.5 nm) laser and XRD were used to investigate the crystalline quality of the Ge. To ensure valid data, settings were constant across all measurements. Figure 4 shows typical Raman spectra of the fabricated GeOIs and bulk Ge wafers. Matching other published data on unstrained GeOIs, sharp Ge-Ge characteristic peaks were found at a wavenumber of 300.29 cm^{-1}, which indicates that no residual strain was formed [18]. The full width at half maximum (FWHM) of the Raman and XRD peak can be used to determine the crystalline quality of the thin film [19]. Raman intensity of the Ge-Ge peak in bulk Ge and GeOI was measured to be 1900.8 and 1831.8 counts, respectively at 300.29 cm^{-1}. The wavenumbers which correspond to the half value of peak intensity are 297.7 and 302.65 cm^{-1} for bulk Ge and 297.41 and 302.87 cm^{-1} for GeOI. Therefore, FWHM values of Ge Raman peak from bulk Ge was measured to be 4.95 cm^{-1}, while that of the lab-made

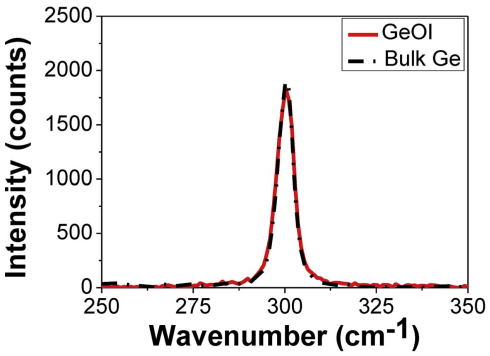

Figure 4. Typical Raman spectra of the fabricated GeOI and Ge wafer.

GeOIs was measured to be 5.46 cm^{-1}. FWHM of GeOI increased by approximately 10% compared to that of bulk Ge. Note that the material quality of Ge layer in the entire thickness of GeOI (i.e., 300 nm) cannot be analyzed by Raman due to the shallow penetration depth at 541.5 nm laser in Ge. A penetration depth of 25 nm was calculated using the absorption coefficient (4×10^5 cm^{-1}) at 541.5 nm. Figure S2 (stacks.iop.org/SST/33/015017/mmedia) shows the XRD peaks measured from the GeOI. The FWHM values of Ge XRD peak from GeOI and bulk Ge were measured to be 124 and 43 arcsec, respectively. Small changes in FWHM of Raman and XRD indicate that the crystal quality of GeOI was degraded due to structural defects such as vacancies and residual H^+ ions associated with H^+ ion implantation. As shown in figure S3 (stacks.iop.org/SST/33/015017/mmedia) the crystal damage created by H^+ ion implantation is more than 100 times smaller than that caused by Boron ion implantation under the same implantation conditions (i.e., dose: $1 \times 10^{17}/cm^2$ and energy: 100 keV) due to the size of ions and their masses. This level of H^+ implantation induced damage has a negligible effect on electrical property of the Ge layer in GeOI [20].

In order to demonstrate functionality of our GeOI as a starting material towards NM transfer based device applications, we fabricated vertical Ge p-n junction diodes by transferring p-type Ge NMs (size: 3 × 3 mm^2) on n-type Ge

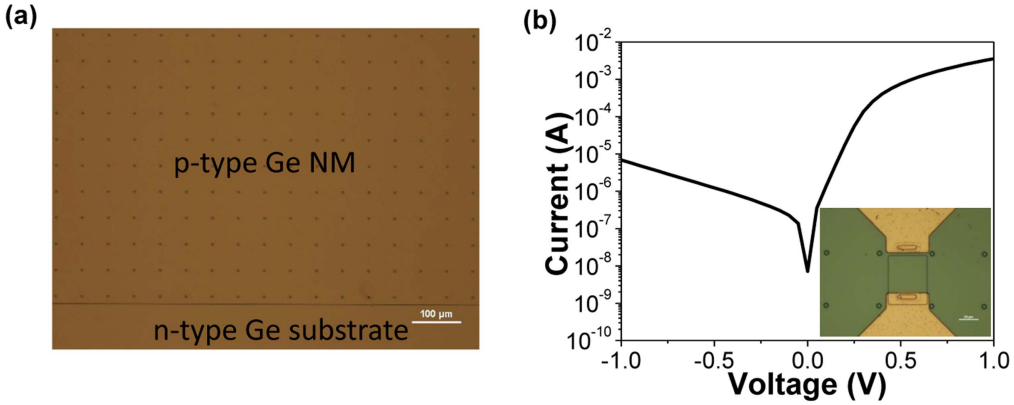

Figure 5. (a) An optical microscopic top-view image of the transferred Ge NM on Ge substrate. Array of etching holes with a diameter of 3 μm and a distance of 50 μm was formed for removal of the underlying BOX. (b) Measured current-voltage characteristics of a Ge vertical p-n junction diode.

substrates (resistivity: $0.005 \sim 0.02\,\Omega$-cm). The Ge NMs were obtained by selective etching of the BOX layer using HF and subsequently transferred via a PDMS stamp. No interface engineering was performed, except for removing the native oxide on receiving Ge substrates by HF. Figure 5(a) shows a top view optical microscopic image of the transferred Ge NM on top of the n-type Ge substrate. The bonded layers were coated with 300 nm of PECVD silicon dioxide (SiO_2) as a passivation layer. The oxide layer was etched for metal contact with p-type and n-type Ge layers, respectively. Ti/Au (10/300 nm) was e-beam evaporated for metal electrodes. The electrical characteristic of Ge-based p-n junction diodes was measured using the semiconductor parameter analyzer (HP4145B). Figure 5(b) shows a current-voltage plot measured under completely dark circumstances. The inset shows a top view microscope image of the fabricated diodes, using a scale bar at 20 μm. A low leakage current of 6.8 μA was measured at the reverse voltage of 1 V. The diode showed a clear rectifying behavior with an on and off current ratio (I_{on}/I_{off}) of ~500 at $\pm$1 V. This demonstrates that our Ge NM can form vertical junctions via a transfer printing method.

Conclusion

In conclusion, we fabricated 4-inch GeOI wafers via a direct wafer bonding and Smart-Cut^{TM} technique. The effect of annealing temperature on exfoliation of the Ge and fracture of the Ge wafer were carefully investigated. It was found that the annealing temperature is a critical factor in avoiding introduction of a fracture in the Ge wafer. Our study shows that annealing at 250 °C for 10 h was the optimum condition for both the complete exfoliation of the Ge layer and preservation of the Ge wafer. Raman and XRD confirmed that similarly favorable crystalline quality of the Ge layer in GeOI was obtained. Demonstration of Ge p-n diodes offers great promise for high performance transferrable Ge NM-based device applications.

Acknowledgments

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